REMARKS

In response to the Final Office Action dated October 20, 2011, and in response to the Request for Continued Examination filed herewith, claims 66-69, 73-76 and 83-85 have been amended. Claims 66-79 and 81-85 are now pending in the application.

In paragraph 3 on page 2 of the Final Office Action, claims 66, 70, 73, 77, 81 -83, and 85 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bowen in view of Ahlin.

In paragraph 4 on page 5 of the Final Office Action, claims 67-69, 71 , 72, 74-76, 78, 79, and 84 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bowen and Ahlin, and in further view of Hoarty.

Applicant respectfully traverses the rejections, but in the interest of expediting prosecution has amended claims.

Independent claim 66 set forth an upgrade interface configured for insertion within an expansion card interface slot of a set top terminal for providing access to a set top terminal microprocessor bus coupled to the set top terminal microprocessor and providing data to the set top terminal microprocessor via the set top terminal microprocessor bus and a hardware upgrade microprocessor, coupled to the upgrade interface, the hardware upgrade microprocessor configured for communicating directly with the set top terminal microprocessor through the set top terminal microprocessor bus via the upgrade interface, wherein the hardware upgrade microprocessor provides enhanced functions to the set top terminal microprocessor through communication with the set top terminal microprocessor using the upgrade interface coupled to the set top terminal microprocessor bus according to

interactive input received from a subscriber, the hardware upgrade microprocessor configured to communicate directly with a headend to receive upgrade data to provide the enhanced functions to the set top microprocessor in response to the interactive input received form the subscriber. Independent claims 73, 83 and 85 set forth similar elements.

In contrast, Bowen merely describes a subscriber terminal that may receive an upgrade device. However, according to Bowen, the set top terminal includes a set top terminal microprocessor and a secure microprocessor. The microprocessor (secure processor 201 of the upgrade device may be coupled directly to the secure microprocessor. However, The microprocessor (secure processor 201) of the upgrade device does not communicate directly with the set top terminal microprocessor. Neither is the microprocessor (secure processor 201) of the upgrade device coupled directly to the set top terminal microprocessor bus. Rather, Bowen states that the secure processor 201 is only coupled to the secure microprocessor bus 143.

Accordingly, Bowen fails to disclose, teach or suggest an upgrade interface providing access to a set top terminal microprocessor bus coupled to the set top terminal microprocessor and providing data to the set top terminal microprocessor via the set top terminal microprocessor bus. While connector 200 electrically extends the control microprocessor memory bus 141 and the secure microprocessor bus 143 to the expansion card 138, Bowen does not suggest that the secure processor 201 is coupled to the control microprocessor memory bus 141. Moreover, Bowen does not suggest that the secure processor 201 communicates with the set top terminal microprocessor 128.

Bowen further fails to disclose, teach or suggest a hardware upgrade microprocessor, coupled to the upgrade interface, the hardware upgrade microprocessor

configured for communicating directly with the set top terminal microprocessor through the set top terminal microprocessor bus via the upgrade interface. As described above, connector 200 electrically extends the control microprocessor memory bus 141 and the secure microprocessor bus 143 to the expansion card 138, but Bowen does not suggest that the secure processor 201 is coupled to the control microprocessor memory bus 141 or that the secure processor 201 communicates with the set top terminal microprocessor 128.

Thus, Bowen fails to disclose, teach or suggest the invention as defined in independent claims 66, 73, 83 and 85, as amended.

Ahlin fails to overcome the deficiencies of Bowen. Ahlin is merely cited as describing a hardware upgrade microprocessor that is configured to communicate with a headend to receive upgrade data to provide the enhanced functions in response to the interactive input from the subscriber.

However, Ahlin fails to disclose, teach or suggest an upgrade interface providing access to a set top terminal microprocessor bus coupled to the set top terminal microprocessor and providing data to the set top terminal microprocessor via the set top terminal microprocessor bus. Ahlin merely describes an upgrade microprocessor communicating with a headend. Ahlin does not suggest that the secure processor 201 communicates with the set top terminal microprocessor 128.

Ahlin further fails to disclose, teach or suggest a hardware upgrade microprocessor, coupled to the upgrade interface, the hardware upgrade microprocessor configured for communicating directly with the set top terminal microprocessor through the set top terminal microprocessor bus via the upgrade interface. As described above, Ahlin merely describes an upgrade microprocessor communicating with a headend. Ahlin does not

suggest that the secure processor 201 communicates with the set top terminal microprocessor 128.

Thus, Bowen and Ahlin, alone or in combination, fail to disclose, teach or suggest the invention as defined in independent claims 66, 73, 83 and 85, as amended.

Hoarty fails to overcome the deficiencies of Bowen and Ahlin. Hoarty is merely cited as disclosing a modem device being provided in an expansion card. However, Hoarty also fails to disclose, teach or suggest an upgrade interface providing access to a set top terminal microprocessor bus coupled to the set top terminal microprocessor and providing data to the set top terminal microprocessor via the set top terminal microprocessor bus. Hoarty merely describes an upgrade device having a modem. Hoarty does not suggest that the secure processor 201 communicates with the set top terminal microprocessor 128.

Hoarty further fails to disclose, teach or suggest a hardware upgrade microprocessor, coupled to the upgrade interface, the hardware upgrade microprocessor configured for communicating directly with the set top terminal microprocessor through the set top terminal microprocessor bus via the upgrade interface. As described above, Hoarty merely describes an upgrade device having a modem. Hoarty does not suggest that the secure processor 201 communicates with the set top terminal microprocessor 128.

Thus, Bowen, Ahlin and Hoarty, alone or in combination, fail to disclose, teach or suggest the invention as defined in independent claims 66, 73, 83 and 85, as amended.

Dependent claims 67-72, 74-79, 81-82 and 84 are also patentable over the references, because they incorporate all of the limitations of the corresponding independent claims 66, 73 and 83, respectively. Further dependent claims 67-72, 74-79, 81-82 and 84

recite additional novel elements and limitations. Applicant reserves the right to argue independently the patentability of these additional novel aspects. Therefore, Applicant respectfully submits that dependent claims 67-72, 74-79, 81-82 and 84 are patentable over the cited references.

On the basis of the above amendments and remarks, it is respectfully submitted that the claims are in immediate condition for allowance. Accordingly, reconsideration of this application and its allowance are requested.

If a telephone conference would be helpful in resolving any issues concerning this communication, please contact Attorney for Applicant, Christopher J. Leonard, at 865-380-5975. If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 13-2725 for any additional fee required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

Merchant & Gould
P.O. Box 2903
Minneapolis, MN 55402-0903
(865) 380-5976

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By: /Christopher J. Leonard/
Name: Christopher J. Leonard
Reg. No.: 41,940